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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/926,364	10/22/2001	Takeo Suzuki	214682US2PCT	9257

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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,364	SUZUKI ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01052005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Receiver with quantizing error reduction".

The disclosure is objected to because of the following informalities:

In page 10 line 25 the recitation "2-1 to 2-4" is incorrect. It is suggested to be changed to "3-1 to 3-4".

In page 12 line 19 the recitation "2-1 to 2-4" is incorrect. It is suggested to be changed to "3-1 to 3-4".

In page 13 lines 22-23 the recitation "2-1 to 2-4" is incorrect. It is suggested to be changed to "3-1 to 3-4".

In page 16 line 24 the recitation "third fourth" is incorrect. It is suggested to be changed to "the fourth".

In page 20 line 13 the recitation "replaced in position" is incorrect. It is suggested to be changed to "swapped in position".

In page 20 line 17 the recitation "every when" is incorrect. It is suggested to be changed to "even when".

Appropriate correction is required.

Claim Objections

Claims 6-10 are objected to because of the following informalities:

In lines 12-13 of claim 6 the recitation "having a bit number modified by the bit number modifier " in lines 12-13 is vague and indefinite because there is insufficient antecedent basis for this limitation in the claim. It is suggested to change claim 6 to

"6. A receiver comprising:

at least one A/D converter which converts a receiving analog signal into a digital signal;

a reduction signal generator which generates a random noise quantizing error reduction signal for reducing a quantizing error of the digital signal converted by the A/D converter;

at least one adder which adds the digital signal and the quantizing error reduction signal generated by the reduction signal generator;

at least one bit number modifier which modifies a bit number of an addition signal added by the adder;

at least one de-spread unit which de-spreads the digital signal having a bit number modified by the bit number modifier;

and at least one integral processing unit which integrates the digital signal inverse infused by the de-spread unit. "

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama (JP 59138118) and further in view of Kaneko (JP 01202038).

As per claim 1 Nakayama discloses an A/D converter (figure 1 block 8) which converts received analog signal into a digital signal; a reduction signal generator which generates a random noise quantizing error reduction signal for reducing a quantizing error of the digital signal converted by the A/D converter (figure 1 block 9); at least one adder which adds the digital signal and the quantizing error reduction signal generated by the reduction signal generator (figure 1 block 10); and at least one low-pass filter which removes a quantizing error reduction signal included in the digital signal having a bit number modified by the bit number modifier (figure 1 block 11). Nakayama doesn't disclose expressly a bit number modifier which modifies a bit number of an addition signal added by the adder. Kaneko discloses a bit number modifier that reduce a bit

number without reducing resolution. Nakayama and Kaneko are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the analog-to-digital converter shaping quantized error disclosed by Nakayama with the bit reduction system disclosed by Kaneko. The suggestion/motivation for doing so would have been to reduce the number of transmission bits without reducing resolution (Kaneko abstract). Therefore, it would have been obvious to combine Kaneko with Nakayama to obtain the invention as specified in claim 1.

As per claim 4 Nakayama and Kaneko disclose claim 1. Kaneko also discloses that the quantizing error reduction signal generated by the reduction signal generator is a rectangular wave signal (figure 1 block 4).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama (JP 59138118) and Kaneko (JP 01202038 A), as applied to claim 1 above, and further in view of Suzuki (JP 09246971). Nakayama and Kaneko disclose claim 1. Nakayama and Kaneko don't disclose expressly that the quantizing error reduction signal generated by the reduction signal generator is a triangular wave signal. Suzuki discloses that the quantizing error reduction signal generated by the reduction signal generator is a triangular wave signal (figure 2C paragraph [0012]). Nakayama, Kaneko and Suzuki are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the analog-to-digital converter shaping quantized error disclosed by Nakayama and Kaneko the triangular wave signal disclosed by Suzuki. The

suggestion/motivation for doing so would have been to provide a high resolution in the analog-digital converter (Suzuki abstract). Therefore, it would have been obvious to combine Suzuki with Nakayama and Kaneko to obtain the invention as specified in claim 2.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama (JP 59138118) and Kaneko (JP 01202038 A), as applied to claim 1 above, and further in view of Kenji (JP 08228152). Nakayama and Kaneko disclose claim 1. Nakayama and Kaneko don't disclose expressly that the quantizing error reduction signal generated by the reduction signal generator is a signal having a high frequency band compared with a frequency band of the receiving analog signal. Kenji discloses that the quantizing error reduction signal generated by the reduction signal generator is a signal having a high frequency band compared with a frequency band of the receiving analog signal (in the applicants' specification background section page 2 lines 11-12) (in the Kenji patent paragraph [constitution and [0011]). Nakayama, Kaneko and Kenji are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the analog-to-digital converter shaping quantized error disclosed by Nakayama and Kaneko the A/D conversion circuit with a quantizing error reduction signal generated by the reduction signal generator having a high frequency band as compared with a frequency band of the receiving analog signal as disclosed by Kenji. The suggestion/motivation for doing so would have been to provide small quantization

errors (Kenji abstract). Therefore, it would have been obvious to combine Kenji with Nakayama and Kaneko to obtain the invention as specified in claim 3.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama (JP 59138118) and Kaneko (JP 01202038 A), as applied to claim 1 above, and further in view of Sawahashi (US 5745531). Nakayama and Kaneko disclose claim 1. Nakayama and Kaneko don't disclose expressly that a matched filter is arranged on the pre-stage of the low-pass filter. Sawahashi discloses that a matched filter is arranged on the pre-stage of the low-pass filter after a digital level corrector and before a low pass filter operating as an envelope detector (figure 1 block 36 column 6 lines 47-55). Nakayama, Kaneko and Sawahashi are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the analog-to-digital converter shaping quantized error disclosed by Nakayama and Kaneko the mached filter as disclosed by Sawahashi. The suggestion/motivation for doing so would have been to provide small quantization errors in spread spectrum systems (Sawahashi abstract and column 1 lines 49-54). Therefore, it would have been obvious to combine Sawahashi with Nakayama and Kaneko to obtain the invention as specified in claim 5.

Claims 6, 7, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama (JP 59138118) and Kaneko (JP 01202038 A), as applied to claim 1 above, further in view of Sawahashi (US 5745531), and further in view of Suzuki (JP 09246971).

As per claim 6 Nakayama and Kaneko disclose claim 1, this is a A/D converter which converts a receiving analog signal into a digital signal; a reduction signal generator which generates a random noise quantizing error reduction signal for reducing a quantizing error of the digital signal converted by the A/D converter; an adder which adds the digital signal and the quantizing error reduction signal generated by the reduction signal generator; and a bit number modifier which modifies a bit number of an addition signal added by the adder. Nakayama and Kaneko don't disclose expressly a de-spread unit which de-spreads the digital signal having a bit number modified by the bit number modifier and a integral processing unit which integrates the digital signal inverse infused by the de-spread unit. Sawahashi discloses a de-spread unit which de-spreads the digital signal having a bit number modified by the digital level corrector and before a low pass filter operating as an envelope detector (figure 1 block 36 column 6 lines 47-55). Suzuki discloses an integral processing unit which integrates the digital signal (figure 1 block 9 paragraph [solution]) this integrator works as a low pass filter for the digital signal. Nakayama, Kaneko, Sawahashi and Suzuki are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the analog-to-digital converter shaping quantized error disclosed by Nakayama and Kaneko the matched filter as disclosed by Sawahashi and the integrator disclosed by Suzuki. The suggestion/motivation for doing so would have been to provide small quantization errors in spread spectrum systems (Sawahashi abstract and column 1 lines 49-54) increasing the resolution of the signal (Suzuki abstract).

Therefore, it would have been obvious to combine Suzuki and Sawahashi with Nakayama and Kaneko to obtain the invention as specified in claim 6.

As per claim 7 Nakayama, Kaneko, Sawahashi and Suzuki disclose claim 6. Suzuki also discloses that the quantizing error reduction signal generated by the reduction signal generator is a triangular wave signal (figure 2C paragraph [0012]). Nakayama, Kaneko, Sawahashi and Suzuki are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the analog-to-digital converter shaping quantized error disclosed by Nakayama and Kaneko the matched filter as disclosed by Sawahashi and the integrator disclosed by Suzuki. The suggestion/motivation for doing so would have been to provide small quantization errors in spread spectrum systems (Sawahashi abstract and column 1 lines 49-54) increasing the resolution of the signal (Suzuki abstract). Therefore, it would have been obvious to combine Suzuki and Sawahashi with Nakayama and Kaneko to obtain the invention as specified in claim 7.

As per claim 8 Nakayama, Kaneko, Sawahashi and Suzuki disclose claim 6. In spread spectrum systems it is inherited that the only way to separate the desired signal from other user signal is using an orthogonal code that the de-spreader will "filter". The quantizing error reduction signal generated by the reduction signal generator have to have an orthogonal code having an orthogonal relation with a spreading code used when the de-spread unit de-spreads the input digital signal.

As per claim 10 Nakayama, Kaneko, Sawahashi and Suzuki disclose claim 6. Kaneko also discloses that the quantizing error reduction signal generated by the reduction signal generator is a rectangular wave signal (figure 1 block 4).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama (JP 59138118), Kaneko (JP 01202038 A), Sawahashi (US 5745531) and Suzuki (JP 09246971), and further in view of Kenji (JP 08228152). Nakayama, Kaneko, Sawahashi and Suzuki disclose claim 6. Nakayama, Kaneko, Sawahashi and Suzuki don't disclose expressly that the quantizing error reduction signal generated by the reduction signal generator is a signal having a high frequency band compared with a frequency band of the receiving analog signal. Kenji discloses that the quantizing error reduction signal generated by the reduction signal generator is a signal having a high frequency band compared with a frequency band of the receiving analog signal (in the applicants' specification background section page 2 lines 11-12) (in the Kenji patent paragraph [constitution and [0011]). Nakayama, Kaneko, Sawahashi, Suzuki and Kenji are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the analog-to-digital converter shaping quantized error disclosed by Nakayama, Kaneko, Sawahashi and Suzuki the A/D conversion circuit with a quantizing error reduction signal generated by the reduction signal generator having a high frequency band as compared with a frequency band of the receiving analog signal as disclosed by Kenji. The suggestion/motivation for doing so would have been to provide small quantization errors (Kenji abstract). Therefore, it would have been obvious to

combine Kenji with Nakayama, Kaneko, Sawahashi, Suzuki to obtain the invention as specified in claim 9.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Young, C.A. "The advantages of strictly digital dither", Advanced A/D and D/A Conversion Techniques and Applications, IEE Colloquium on , 8 May 1989 Pages:2/1 - 2/3. Wagdy, M.F. "Effect of additive dither on the resolution of ADCs with single-bit or multi-bit errors". Instrumentation and Measurement Technology Conference. 1995. IMTC/95. Proceedings. 'Integrating Intelligent Instrumentation and Control'., IEEE , 24-26 April 1995. Pages: 802.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAT 1-5-2005

M. G

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER